Fundamentals of Timing Devices

1. Introduction

“Timing devices” proposes a new way to investigate brains. An individual timing device acts like a neuron and an assembly of timing devices performs specific brain-like functions. The resemblances are imperfect because timing devices are idealized mental constructs. The author suggests that, despite the defects, timing devices identify principles that can guide investigations into actual brains. The Ideal Gas Law (pV=nRT) is a similar mental construct.

Designs for timing device assemblies look like schematic diagrams used in standard electronic circuits. In circuit diagrams, iconic symbols stand for electronic components that come from a "kit of parts" made up of physical devices. A person builds an electronic circuit by taking parts from the kit and connecting the parts according to a schematic diagram for the circuit. The electronic kit of parts has a "core" that includes resistances, capacitances, signal sources, diodes and bipolar junction transistors. Core parts are used to make up circuits and modules that generate and process important classes of signals, e.g., sine waves and their combinations. Additional devices such as photo-sensors and memory devices supplement the core.

The features of standard electronic circuits described in the preceding paragraph re-appear in the timing devices system. At this time, the core members of the timing devices kit of parts are:

1. the primal timing device;
2. the gate normally open timing device;
3. the gate normally closed timing device;
4. the two-pulse trigger timing device; and
5. the difference device.

This presentation of the core timing devices is developmental. The primal timing device is a minimal unit and is the point of origin. The step from the primal device to the gate normally open device resembles the step from the semiconductor diode to the bipolar junction transistor (pnp or npn). Development of later devices involves further additions and modifications.

All devices and designs are conceptual; there are no plans for working models.

A tabular form is used to integrate the presentation of the five core timing devices. The author suggests that the integrated tabular form provides a solid foundation for further development of the timing devices system.

2. Timing device signals

Signals in timing devices have a form that is different from that of signals in standard electronic circuits. The basic unit is a "pulse" that carries a specific amount of energy. In the ideal system, a pulse is instantaneous both in duration and in transmission. It is a sudden event appearing in a quiescent background. The pulse form idealizes the "spike" or "action potential" seen in nerves. The pulse is a unit that is "the same" in all timing device signals and that is the sole constituent of all such signals. In other words, all content of signals in the timing devices system is conveyed in and through temporal patterns of uniform pulses.

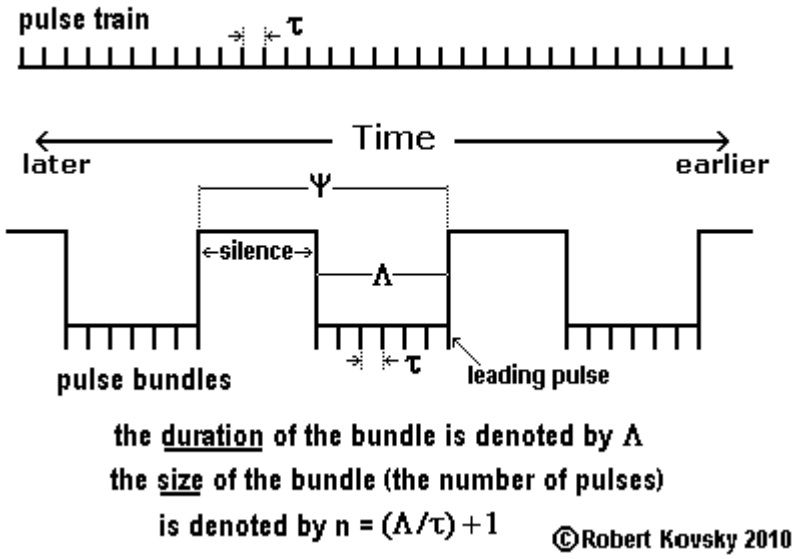
Some timing device signals are perfectly repetitive or ideal pulse patterns. In addition, there are various approximations to the ideals, as well as signals that change during operating processes. Designs for units that generate and process ideal pulse patterns are easiest to understand and provide useful points of origin for further development.

Two ideal pulse patterns are shown in Figure 1, along with definitional terms.

(1) pulse trains – the signal is a series of pulses; the "period" or duration of time between successive pulses is always "the same," a uniform period typically denoted by τ; and

(2) pulse bundles – the signal is constructed from two pulse trains as follows (see Figure 1): one pulse train, ψ, has the longer period; the pulse expressing the ψ pulse train, called the "leading pulse," is the first of several pulses in the "pulse bundle" in which pulses are separated by the uniform shorter period, τ; then, there is silence for the rest of the ψ cycle; and the pattern is repeated "the same" during each ψ cycle.
Each ψ cycle has a bundle of pulses with a duration Λ and a silent part. In the ideal signal, each bundle has the same number of pulses or "size," n; and $n=(\Lambda/\tau) + 1$. Three "values" define a pulse bundle: ψ, Λ and τ. Such values are useful even when the signal is only an approximation to an ideal, e.g., when it has a variable pattern.

Figure 1: ideal timing device signals are repetitive pulse patterns

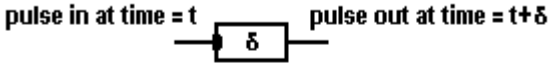


3. The Primal Timing Device

Figure 2 shows operations of the primal timing device.

Suppose a pulse arrives at the device at a time "t" as measured on a reference clock. The function of the device is to discharge a pulse at time "t+δ." The device is unresponsive to a second input pulse from time t until a later time, t+(δ+β). δ and β are "timing intervals" that specify the primal timing device (like ohms specify a resistance).

Figure 2: operations of the primal timing device



if a pulse arrives at time t, the timing device is unresponsive until t+(δ+β).

δ and β, *timing intervals*, are the specifications of the primal timing device.

δ is called the *responding period*.

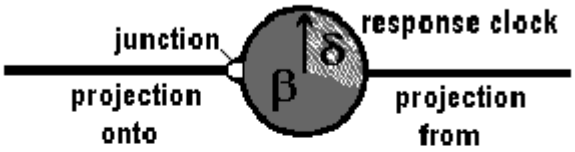
β is called the *refractory period*.

The timing interval δ is called the "responding period" and is the fundamental unit in timing device operations. The timing interval β is called the "refractory period" and can be important or unimportant, depending on the application.

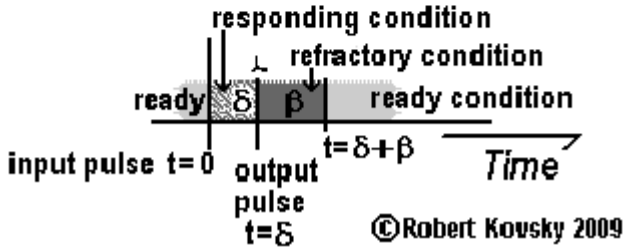
Figure 3 shows the primal timing device and its operations in more detail. The chief part of the primal timing device is a "response clock" that is like a stopwatch used in sports contests, shown in Figure 3.a as a circular clock dial. Two "projections" connect the primal timing device to other timing devices. A "projection from" carries pulses away from the timing device. A "projection onto" carries pulses to the timing device. A "junction" connects the projection onto to the response clock. A pulse through the junction starts the "response process," which runs through a cycle of "conditions," during which a pulse is discharged.

Figure 3: details of primal timing device

a. primal timing device in ready condition



b. cycle of conditions in a response process



As shown in Fig. 3.b, a primal timing device has a "ready condition," a "responding condition" and a "refractory condition." The device responds to an incident input pulse only when it is in the ready condition. In Fig. 3.b, an input pulse reaches a ready device at time t = 0, initiating the response process. The response clock starts and the device enters into the responding condition. At t = δ, the device discharges an output pulse on the projection from; and the device enters into the refractory condition; and that condition continues until t = δ + β, when the device enters into the ready condition, completing the response process.

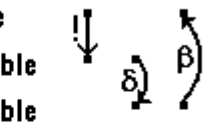
This presentation of five core timing devices employs a tabular form to show the conditions of a timing device and the changes in conditions in an organized way.

Table 1 lists the conditions and changes for the primal timing device and shows the formal element for schematic designs.

The responding and refractory conditions are unstable; and changes are caused by the response clock according to the internal timing intervals. The stable ready condition changes only as a result of an input pulse, called a "trigger input pulse" in anticipation of additional inputs later. There are no changes in conditions other than those listed. A pulse is discharged when the responding condition changes to the refractory condition but the discharge is not shown on the Table.

Table 1: primal timing device

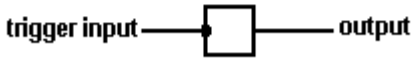
conditions	type	changes
ready	stable	
responding	unstable	
refractory	unstable	



! —— trigger input pulse

δ, β – internal timing intervals

formal element for schematic designs



The change caused by the trigger input pulse is symbolized by a straight-line exclamation point or "bang" and the changes caused by internal timing intervals are symbolized by curved arrows.

Each timing device is functionally defined by a "set of rules" involving conditions and changes in conditions. Rules specify inputs and timing intervals that control changes in conditions.

Rules for the primal timing device are: Incident trigger input pulses can occur at any time, but the timing device is responsive to such pulses only when it is in the ready condition. A trigger input pulse changes the ready condition to the responding condition. In the responding condition, the device awaits the discharge of an output pulse and the change to the refractory condition at a specific time in the future. In the refractory condition, the device awaits a change to the ready condition at a specific time in the future.

There is no specific "internal mechanism" or "internal activity" that describes or embodies the operations or rules of the primal timing device. Different kinds of "internal mechanisms" or "internal activities" might describe or embody such operations.

The operations of the primal timing device impose a "constraint" on the arrival rate of incident pulses. If the device is to respond to each incident pulse, pulses must arrive slowly enough for the response process to completely cycle and return the device to the ready condition between pulses. A standard for performance is the generation of output that is identical to input, except for a delay. To achieve this performance, there must be a "minimum period" between any two pulses in the input pulse train, denoted by "τ_{MIN}." For the primal timing device $\tau_{MIN} = (\delta + \beta)^{+}$. The superscript "+" means "plus an infinitesimal bit more." That is, if a period greater than $\tau=(\delta + \beta)$ intervenes between two successive pulses, both pulses will "pass through" the primal timing device. If $\tau < (\delta + \beta)$, the device will fail to respond to all of the pulses.

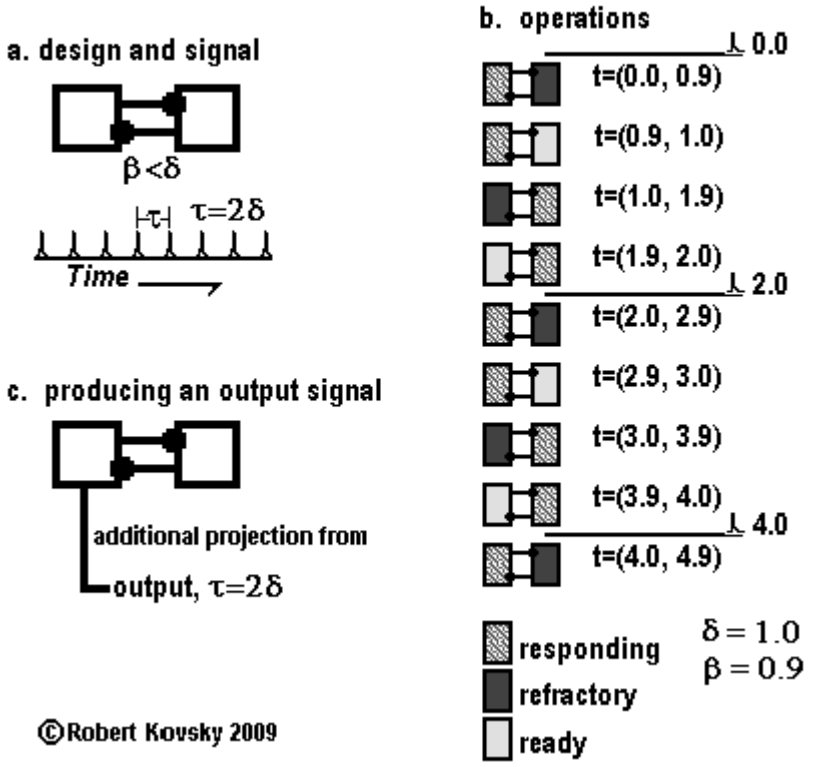
4. Connecting timing devices, an application

Figure 4.a shows two primal timing devices connected together and operating as a signal generator. Each timing device's projection from is "connected" or "spliced" to the projection onto of the other timing device; pulses discharged by one arrive instantaneously at the other. The two primal timing devices have identical δ and β; and $\beta<\delta$. The signal in each projection is a steady stream of pulses with a period of 2δ.

Details of operations are shown in Figure 4.b: at the top, one timing device discharges at t=0.0. That timing device then discharges repeatedly at t=2.0, 4.0, etc. as part of the cyclical activity of the two devices. Time measurements refer to a standard or laboratory clock. The time dimension can be measured using any quantity, e.g., minutes, seconds, milliseconds.

In Figure 4.c, another projection from is added to one of the timing devices in the signal generator to serve as an "output" line. Whenever that timing device discharges, the pulse appears on the output line as well as on the projection from that timing device that goes to the other timing device. The output signal is an ideal pulse train with a period of 2δ.

Figure 4: two interconnected primal devices generating a signal



The addition of the projection from in Figure 4.c is an example of a general rule called the "equal output rule." Under the rule, any number of projections from can be added to a timing device and each projection from carries an identical signal. Additionally, a projection from can branch and turn into multiple projections onto that can trigger multiple timing devices. An equal and identical signal arrives at each timing device through that device's projection onto.

5. The Gate Normally Open Timing Device

The gate normally open device, shown in Figure 5, is developed from the primal timing device by adding features and modifying features. The step from the primal device to the gate device is comparable to the step from a semiconductor diode to a bipolar junction transistor.

The gate normally open device is closely related to the gate normally closed device discussed in the next section. Figure 5.a shows added features of both gate devices: a "modulation junction" that receives "modulation input" pulses produced by other timing devices through projections from those devices. Input modulation pulses operate a "gate" embodied in the device. The gate has a status that is either "open" or "closed." When the gate is open, the device responds to trigger input pulses exactly like a primal timing device. When the gate is closed, the device is unresponsive and no output pulses are generated from trigger input pulses.

Figure 5: the gate normally open timing device

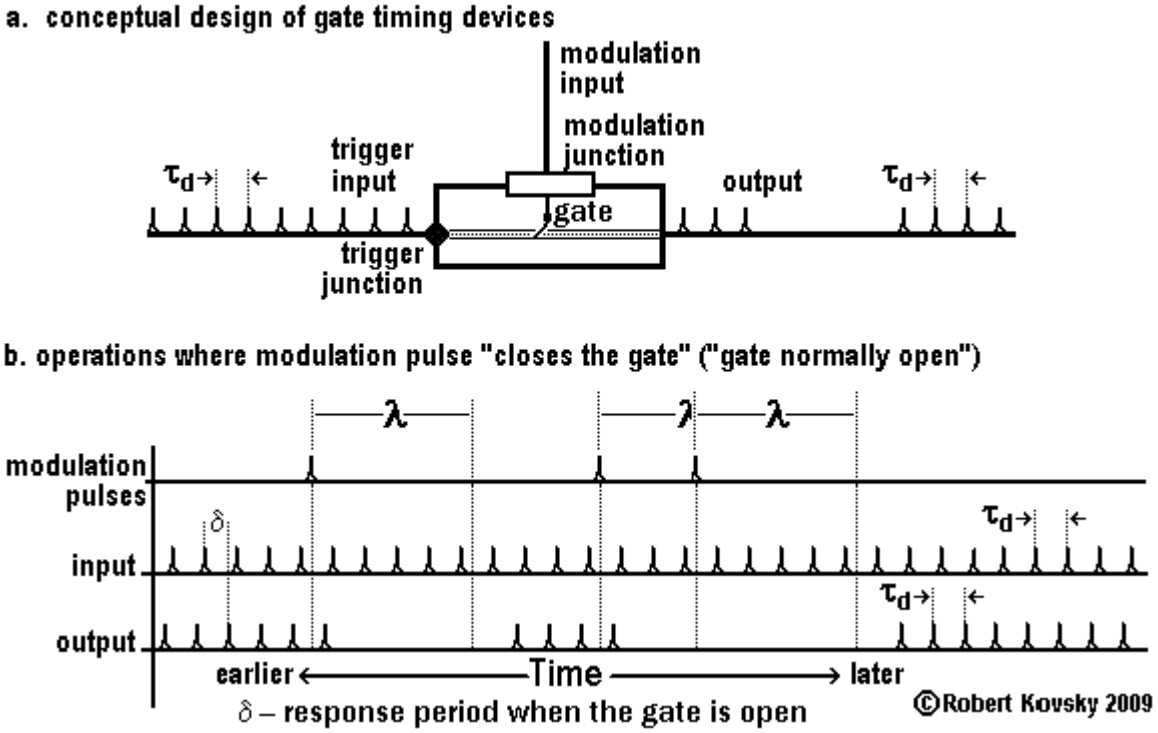
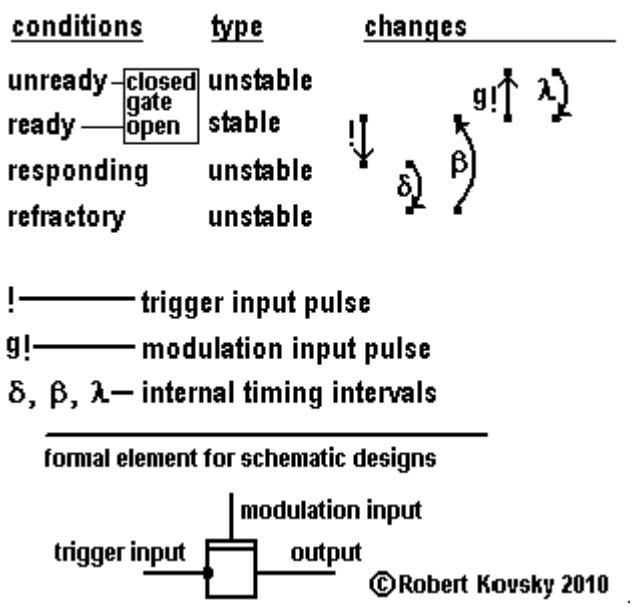


Figure 5.b illustrates operations of the gate normally open timing device. A "gate process" runs both the gate and a "gate clock," which operates like the response clock but independently. If the normally open gate device is in the ready condition, a modulation pulse starts the gate clock and gate process; the gate process immediately closes the gate while the gate clock runs for a period of time, denoted by λ, the "gate period." While the gate process is running, the device is unresponsive to trigger input pulses. After the gate period expires, the gate process returns the device to the ready condition, re-opening the gate. If the gate process is running when another modulation pulse arrives, the gate clock re-starts at 0. If a modulation pulse arrives while the response process is running, the gate clock starts immediately but the gate process waits until the response process completes its cycle and the device returns to the ready condition before closing the gate, avoiding any interference between the processes.

Table 2 shows the conditions and changes for the gate normally open timing device. Table 2 is developed from Table 1 for the primal timing device by adding and modifying features.

Additional features – the "unready" device condition, the independent "gate process," the "gate" and the "gate clock" – are connected with the primal timing device through a shared ready condition. The gate has a "status" that is either "closed" or "open" at any instant. The gate process is a cycle made up of the new unready condition, an input modulation pulse (denoted by "g!") that changes the condition from ready to unready and the "gate period," denoted by "λ," that is the specification of the gate clock used by the gate process to open the gate and change the device condition from unready to ready.

Table 2: gate normally open timing device



For the response process, the cycle of conditions is "ready–responding–refractory–ready." The cycle of conditions for the gate process is "ready–unready–ready." Should both processes be running at the same time, co-ordination is needed to avoid interference.

Here, interference is avoided by inserting a delay in the closing of the gate. Suppose a trigger input pulse arrives when the device is ready. While the response process is ongoing, a modulation input pulse arrives. The modulation input pulse starts the gate process and the gate clock but actual gate closure is delayed until the device returns to the ready condition. At the first instant that the device returns to the ready condition after the conclusion of the response process, the gate process changes the condition of the device to unready and closes the gate, changing the gate status. The gate clock continues to run. Because the device is unresponsive throughout the response process, the gate can be closed at any instant during that process without affecting operations and interference is avoided by closing it, in effect, at the final instant of response process (or, more precisely, at the next instant thereafter).

In the gate normally open timing device, as in the primal timing device, there is a set of rules. The rules for the gate normally open device involve conditions "unready," "ready," "responding" and "refractory" that are functionally defined by the interactivities (or lack thereof) of the timing device, by input pulses and by the timing intervals that schedule future events. While in the unready condition, the device is awaiting a change to the ready condition at a specific time in the future, subject to extension should another modulation input pulse arrive. The ready condition is stable but can be changed by pulses through either the trigger input or the modulation input. The device is responsive to trigger input pulses only when it is in the ready condition but it is always responsive to modulation input pulses that start or extend

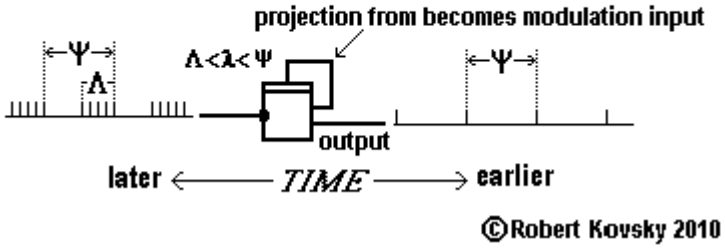
the gate process. As with the primal device, the unstable responding condition is awaiting the discharge of a pulse and the change to the refractory condition at a specific time in the future. The unstable refractory condition is awaiting a change to the ready condition at a specific time in the future. The status of the gate does not change during the responding period or the refractory period but, as noted above, only when the device is in the ready condition, so there is no interference between the processes.

Figure 6 shows an application of the gate normally open timing device, where the function of the arrangement is to extract the leading pulses from a signal of pulse bundles. (See Figure 1.) The device has two projections from, which operate according to the "equal output rule." (See § 4.) One projection from is labeled "output" and carries the signal to further timing devices; and the other projection from is "spliced to" or "connected to" the modulation input. The discharge of a pulse by the device immediately closes the gate as to subsequent pulses, but only for a limited time, the modulation period, λ. After λ expires, the gate opens and the device is again responsive to an input pulse.

When a pulse bundle with a duration that is less than λ is incident on the trigger input, the first pulse triggers the response process but the first discharge becomes a modulation pulse that closes the gate to all later pulses in the bundle.

This application requires that λ be greater than Λ so that the gate is closed for the entire bundle. For the device to become ready to respond to the first pulse of the subsequent bundle, λ must be less than ψ. Hence, to extract the leading pulse from each bundle, Λ<λ<ψ.

Figure 6: application, gate normally open timing device extracting leading pulses from pulse bundles



6. The Gate Normally Closed Timing Device

Operations of the gate normally closed timing device are shown in Figure 7. The operations closely resemble those for the gate normally open timing device but with modifications. The device is "normally" unresponsive to trigger input pulses. A modulation pulse opens the gate for the gate period, during which the device responds exactly like the primal timing device.

Figure 7: gate timing device, gate normally closed

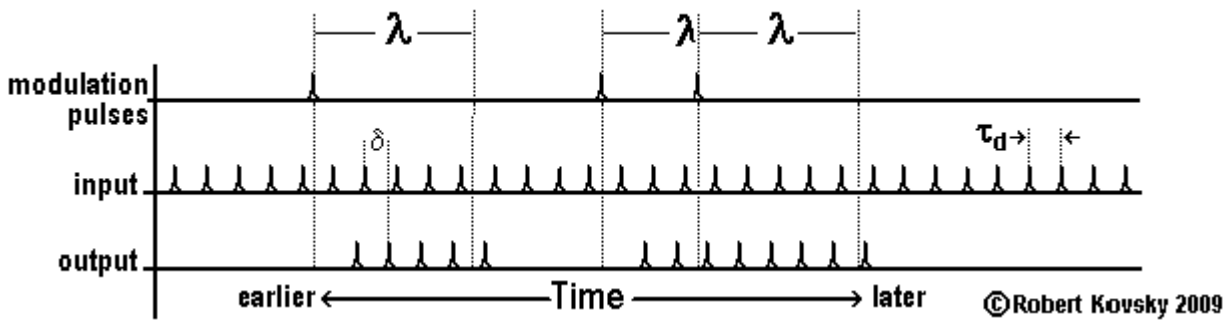
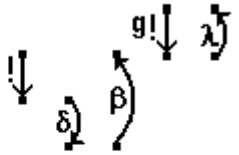


Table 3 continues the development of the integrated tabular form used for core timing devices. Table 3 is developed from Table 2 by way of modifications. The gate and gate clock are the same as that used in the gate normally open device. The modified gate process is a variant of the prior form with specific detailed modifications as follows:

Compared to the gate normally open timing device, there is a reversal of directions of changes caused by an input modulation pulse (g!) and expiration of the gate period (λ): now the input modulation pulse opens the gate and the expiration of the gate period closes the gate. In this device, the ready condition is unstable and the unready condition is stable – this is a modification of both the primal timing device and the gate normally open timing device.

Table 3: gate normally closed timing device

conditions		type	changes
unready	closed gate	stable	
ready	open	unstable	
responding		unstable	
refractory		unstable	

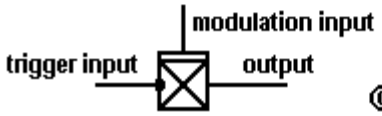


! ——— trigger input pulse

g! ——— modulation input pulse

δ, β, λ — internal timing intervals

formal element for schematic designs



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In the customary way, the set of rules for the gate normally closed timing device is stated in terms of the four conditions, the responsiveness of each, and the changes between conditions controlled by the response clock and the gate clock and by trigger input and modulation input.

Like the previous devices, the gate normally closed timing device is responsive to a trigger input pulse only when it is in the ready condition. Device operations involved in the change

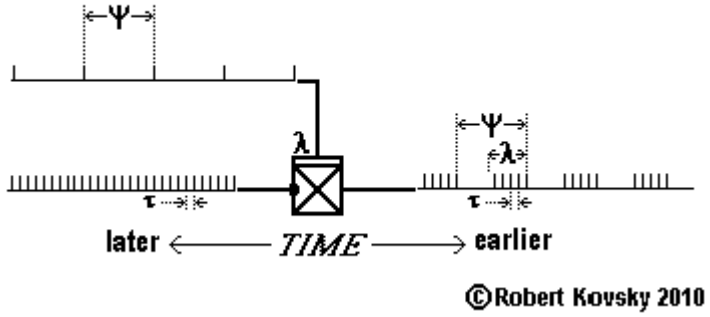
from the responding condition to the refractory condition are identical with the primal device. Device operations involved in the change from the refractory condition to the ready condition are also identical with the primal device. There is a delay in closing the gate while the response process is running, as in the gate normally open timing device discussed in § 5.

In the gate normally closed timing device, the stable unready condition, with a closed gate, is changed only by the arrival of a modulation pulse that triggers the gate process, changing the device condition to ready, starting the gate clock and opening the gate. The gate clock runs until λ expires. If the device is in the ready condition when λ expires, the gate process closes the gate, changing its status, and resets the gate clock to await a modulation input pulse. If the device is in the responding or refractory condition when λ expires, the gate process delays closure operations until the response process returns the device to the ready condition.

The device is always responsive to a modulation input pulse; that is, a modulation pulse will start or extend the gate process and start or re-start the gate clock.

Figure 8 shows an application of the gate normally closed timing device, namely, generating pulse bundles from two input pulse trains. (See §§ 2, 4.) A longer-period pulse train period ψ arrives through the modulation input and a shorter-period pulse train with period τ arrives through the trigger input. Each modulation pulse opens the gate for λ and the device generates a bundle of pulses. The duration of the pulse bundle – the time interval from the first pulse to the last pulse denoted $\Lambda=(n-1)\tau$ – is generally not equal to λ. Rather $(n-1)\tau \leq \lambda \leq n\tau$.

Figure 8: application, gate normally closed timing device generating pulse bundles



7. The Two-Pulse Trigger Timing Device

Figure 9 shows a timing device that is governed by the "two-pulse trigger rule." The rule is that two input pulses are required to trigger the response process and start the response clock; and both pulses must arrive at the timing device within a timing interval, ξ, called the "readiness period." A "readiness process" and a "readiness clock" are incorporated into the device.

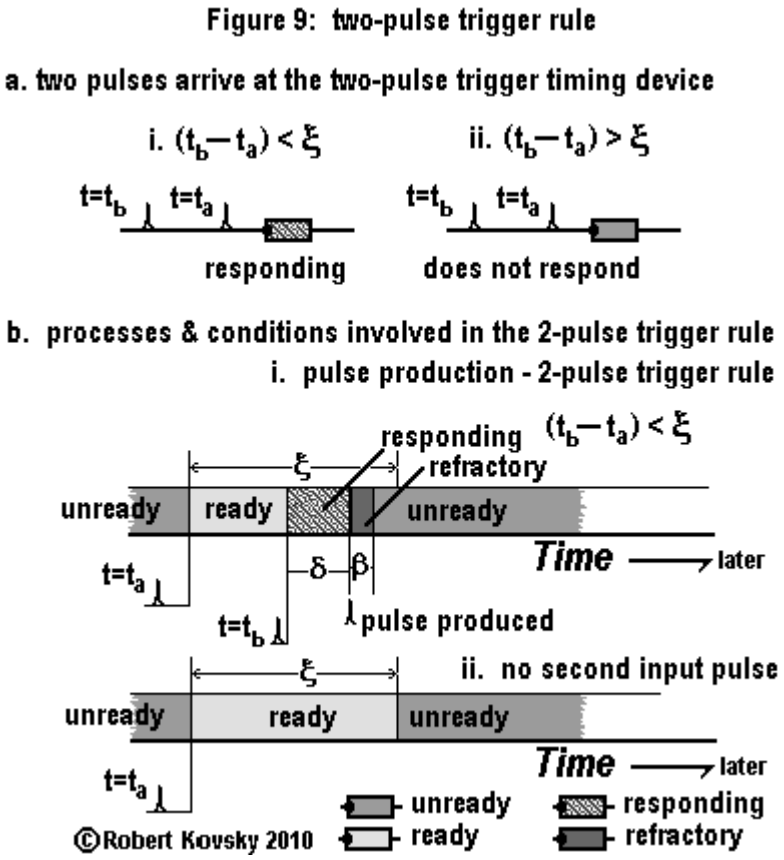


Figure 5.a shows the two-pulse trigger rule. A pulse arrives at $t=t_a$ and a second pulse arrives at $t=t_b$. If the difference in time of arrivals is less than ξ, i.e., if $(t_b - t_a) < \xi$, the response process starts. On the other hand, if $(t_b - t_a) > \xi$, there is no response.

Fig. 5.b shows the conditions involved in the two-pulse trigger rule in greater detail. The "unready condition" is stable. The ready condition is unstable and lasts only for a maximum of ξ, the readiness period. A first trigger input pulse changes the unready condition to the ready condition.

The readiness process operates in a cycle, changing the device condition from unready to ready and back again. The readiness clock operates like prior clocks with independent start, stop and timing interval. If a two-pulse trigger rule timing device is in the unready condition and a trigger input pulse arrives, the device condition changes to the ready condition and the readiness clock starts. If the timing device is in the ready condition, a second input pulse triggers the response process, starting the response clock and changing the device to the responding condition. The readiness process terminates and the readiness clock stops and is reset. (See Fig. 5.b.i.)

If the ready condition continues for the full readiness period of ξ without the arrival of a second pulse, the ready condition terminates and the timing device returns to the unready condition. The readiness clock awaits another input pulse. (See Fig. 5.b.ii.)

[In prior publications, conditions in the two-pulse trigger device were given different names. What is here called the "ready" condition was previously called the "roused" condition, the "unready" condition was previously called the "ready" condition. Also, the "readiness clock"

was previously called the "rousal clock." Only names are changed.]

Table 4 for the two-pulse trigger device is developed from Table 1 for the primal timing device.

The stable unready condition is added to Table 1 while the ready condition is modified to be an unstable condition, as in Table 3. The readiness process, readiness clock and two new changes of conditions are added, namely, a change from unready to ready caused by a trigger input pulse and a change from ready to unready caused by the readiness process after expiration of the readiness period, ξ, on the readiness clock. The change from the refractory condition is modified and is now a change from the refractory condition to the unready condition.

Table 4: two-pulse trigger device

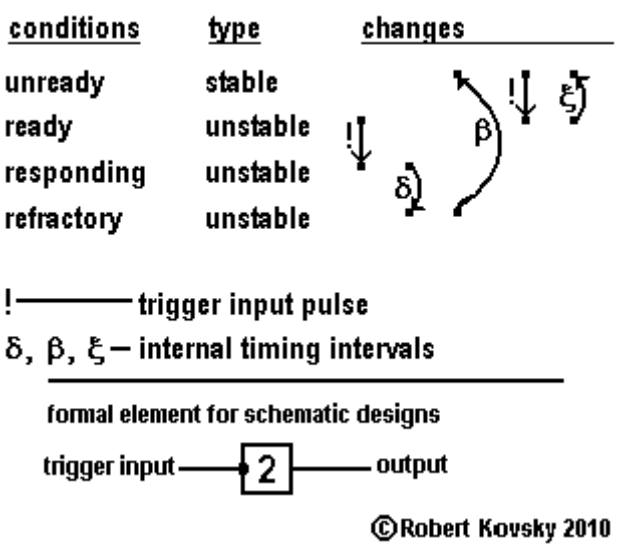
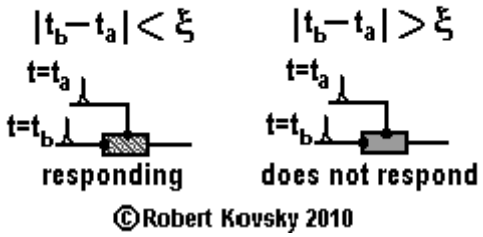


Table 4 shows resemblances to and differences from Table 3 for the gate normally closed timing device. The types of conditions, stable or unstable, are the same in the two devices. In each device, a first input pulse is necessary in order for a second input pulse to start the response process and lead to the discharge of an output pulse. The big differences are that the change from the refractory condition has been modified and that the only input in the two-pulse trigger device is trigger input. The two-pulse trigger device does not need a gate. There is no possible question of interference between the readiness process and the response process.

Suppose an ideal pulse train with period τ is incident on the device shown in Figure 9 and that $\tau > \tau_{MIN} = (\delta+\beta)^{+}$. ($\tau_{MIN}$ is discussed in § 3.) Generation of output pulses requires operating the device within the constraint $\tau < \xi$. If $\tau > \xi$, the readiness period will end before a second pulse arrives. When the device is generating output, one pulse in the input pulse train changes the unready condition to the ready condition and the following pulse changes the ready condition to the responding condition. Two input pulses lead to one output pulse. For an incident ideal pulse train, $\tau < \xi$, the two-pulse trigger device generates an ideal output pulse train with period 2τ.

Figure 10 shows a two-pulse trigger timing device with two projections onto that can receive trigger input pulses. The rule is that the arrival of two trigger input pulses through either projection onto within the readiness period ξ will cause the device to respond. It doesn't matter which pulse arrives first. The statement of the two-pulse trigger rule is modified to employ the absolute value of the difference of time of arrivals. An output pulse will be discharged if $| t_b - t_a | < \xi$.

Figure 10: two-pulse trigger timing device with two projections onto



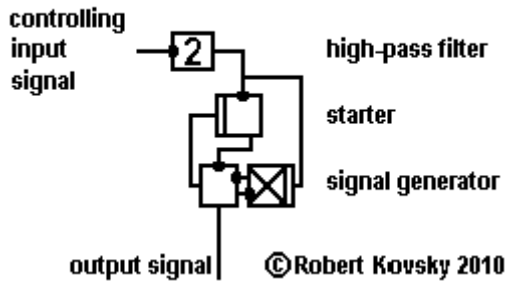
In contrast to the arrangement in Figure 9, arrivals in the arrangement in Figure 10 can occur simultaneously, or nearly so. Some useful devices employ a ξ less than δ.

In devices other than the two-pulse trigger device, multiple projections onto are governed by the "one-pulse trigger rule," namely, that an incident trigger input pulse through any projection onto causes a ready device to respond. The "one-pulse trigger rule" is the default. Trigger rules for multiple projections onto are complements to the "equal-output" rule for multiple projections from discussed in § 4.

Figure 11 shows an assembly of timing devices that combines all of the previous timing devices and that functions as a "controlled signal generator." The "controlling input signal" is a pulse train (or a close approximation), with a period between pulses that is keyed to ξ, the readiness period of the two-pulse trigger device, as discussed in connection with Figure 9. The device is acting like a "high-pass filter" in standard electronic circuits. When the period between pulses in the controlling input signal is less than ξ, the two-pulse trigger device delivers pulses to other devices in the assembly; if pulses in the controlling input signal arrive with a period between them greater than ξ, no such pulses are delivered.

The "signal generator" in Figure 11 is based on the design in Figure 4 that uses two primal timing devices. In Figure 11, one of the timing devices in the signal generator is a gate normally closed timing device. The λ for this device is several times the ξ of the two-pulse trigger timing device so the signal generator maintains operations as long as the two-pulse trigger device is generating output. If such output ceases, the signal generator shuts down.

Figure 11: start/stop for signal generator



The gate normally open device labeled "starter" in Figure 11 is developed from Figure 6. Suppose the signal generator has been silent and the gate normally open device is open. The "first pulse" generated by the two-pulse trigger device both triggers the starter device, starting the signal generator, and opens the gate in the gate normally closed device. The ungated device in the signal generator discharges pulses into the modulation junction of the gate normally open device, closing its gate and keeping out "extraneous pulses" that might roughen pacing of the signal generator.

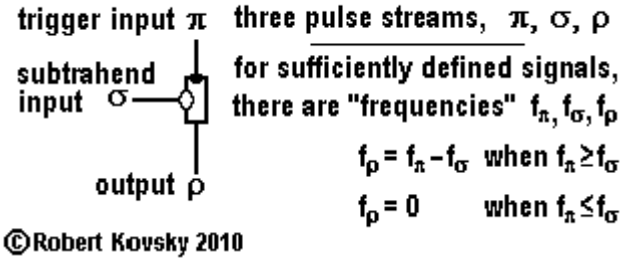
In sum, the signal generator is "on" when the frequency of pulses in the controlling input signal is above $1/\xi$ and the signal generator is "off" when the frequency of pulses is less $1/\xi$. This design is an efficient way to control signals in brain-like assemblies of timing devices.

8. The Difference Device

Figure 12 shows the difference device. There are three signals or pulse streams: the trigger input π, the subtrahend input σ and the output ρ.

Suppose trigger input pulses arrive with a frequency f_π and subtrahend input pulses arrive with a lower frequency f_σ; then, output pulses in the ρ signal are generated with a frequency of:
$f_\rho = f_\pi - f_\sigma$.

Figure 12: difference device

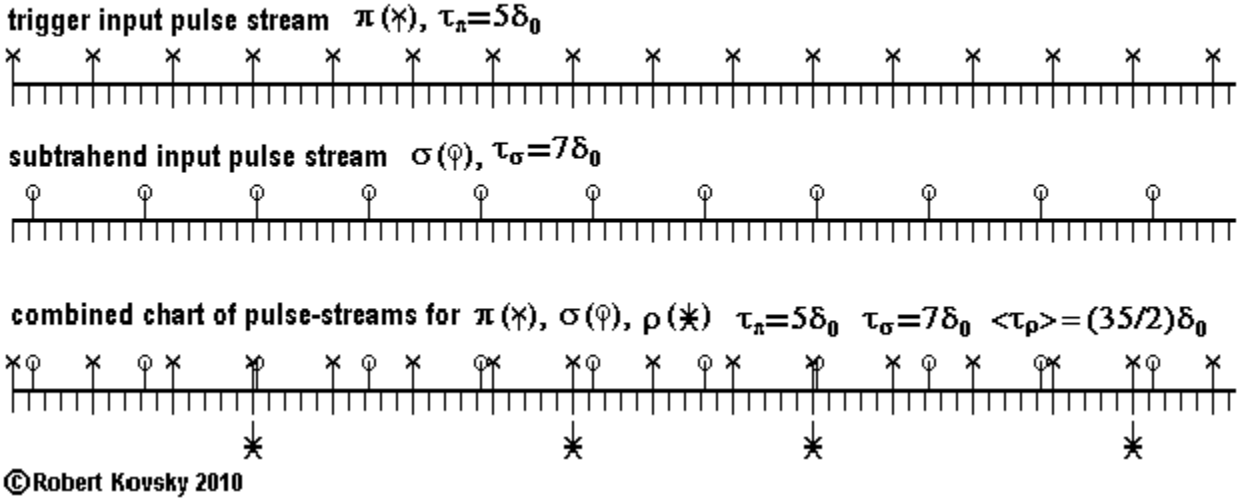


Output is generated from the difference device only if $f_\pi \geq f_\sigma$. If $f_\pi \leq f_\sigma$, there is no output, $f_\rho=0$.

The "difference" in the difference device is the subtraction of pulses in one input pulse stream from pulses in another input pulse stream to get a resulting stream.

Figure 13 shows operating details for a particular example of trigger input and subtrahend input signals. Both input signals are ideal pulse trains. Trigger input pulses have a period of $5\delta_0$ between them and subtrahend input pulses have a period of $7\delta_0$. The output pulse stream, with an average pulse rate of $35/2\delta_0$, has an irregularity with alternating periods of $20\delta_0$ and $15\delta_0$; it is thus only an approximation to an ideal signal. The approximation will work in many applications but there are also applications where the approximation will fail.

Figure 13: operational example for the difference device



A "cancellation principle" is operating in the difference device. Each subtrahend pulse "cancels" one trigger input pulse. When two trigger pulses arrive without an intervening subtrahend pulse, the second trigger pulse is not "cancelled" but causes the discharge of an output pulse. If three trigger pulses arrive without an intervening subtrahend pulse, the second

and third trigger pulses cause two output pulses to be discharged and so forth.

There is a constraint on the pulse streams, namely, that two or more subtrahend input pulses may not arrive between two trigger input pulses. If the pulse streams satisfy the constraint, the output pulse frequency will, on average, exactly equal the input trigger pulse frequency minus the subtrahend pulse frequency. If the pulse streams violate the constraint, the output frequency will be greater than the exact difference of averages. Signals that satisfy the constraint are "sufficiently defined" for proper operations.

Table 5 for the difference device continues development of tabular forms, combining features from multiple Tables for prior devices. For clarity, discussion is primarily based on Table 1 for the primal timing device with secondary comparisons to other developed timing devices.

To develop the primal device into the difference device, a stable unready condition is added and the ready condition is modified to become unstable. A chief added feature is a "counter," a physical device part with a status of either zero or one. Generally, the status of the counter is zero when the device is in the unready condition and the status is one when the device is in the ready condition, responding condition or refractory condition. Device conditions and the status of the counter can be changed in multiple ways, including a "waiting process" that operates independently of the primary response process in ways resembling those of previously-discussed processes and that uses a "waiting clock and" a "waiting period," ξ.

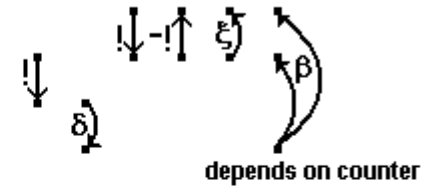
The waiting process is started or re-started (and extended) by the arrival of a trigger input pulse and terminates when the device returns to the unready condition.

The status of the counter is changed by a trigger input pulse when the device is unready, by a subtrahend pulse at any time or by a return to the unready condition after expiration of ξ.

The change in condition from the refractory condition is modified so that it depends on the status of the counter.

Table 5: difference device

conditions		type	changes
unready	zero counter	stable	
ready	one	unstable	
responding		unstable	
refractory		unstable	

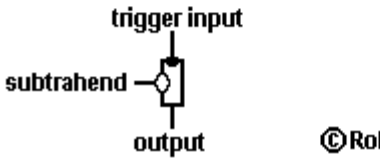


!——— trigger input pulse

-!——— subtrahend pulse

δ, β, ξ— internal timing intervals

formal element for schematic designs



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The timing interval ξ, the "waiting period" is relatively long. It starts fresh upon the arrival of each trigger input pulse, returns the device to the stable unready condition after inputs have ceased and is nonfunctional during active operations. While inputs are active, alternations between the unready and ready conditions are caused by input pulses, not by a process. Input pulses and changes to the status of the counter can occur at any time, including changes caused by subtrahend pulses arriving during the response process.

The set of rules for the difference device are as follows. If the device is in the unready condition and the status of the counter is at zero when a trigger input pulse arrives, the waiting process starts, the status of the counter is changed to one and the device condition changes to the ready condition. If the device is ready (and the counter is at one) when a subtrahend pulse arrives, the counter changes to zero, the waiting process terminates and the device condition changes to the unready condition. If the device is ready (and the counter is at one) when a trigger input pulse arrives, the counter remains at one and the device cycles through the response process, as in the primal device, and returns to the ready condition. Subtrahend pulses change the status of the counter to zero regardless of the condition of the device. When the refractory period expires, the refractory condition changes to the unready condition if the status of the counter is zero and to the ready condition if the status of the counter is one.

Nothing happens to the device if the status of the counter is zero and a subtrahend pulse arrives. The result is the same as if no pulse arrives. If an exact "difference frequency" is to be generated, this course of events is a failure of the device to operate as desired or an "error."

To avoid such errors, the input signals must conform to the constraint that the period between subtrahend input pulses is greater than the period between trigger input pulses, or $\tau_\sigma > \tau_\pi$. Then at least one trigger input pulse will arrive between any two subtrahend input pulses. The constraint is applied on a moment-to-moment basis but becomes $f_\pi > f_\sigma$ for well-defined signals.

Figure 14 shows how an error is generated when operations are in violation of the constraint. The average frequencies of the input pulse streams are the same as in Figure 13 but the pulses arrive in pairs. A pair of trigger input pulses arrives when the counter is at 0 and generates a single output pulse. Typically, a pair of subtrahend input pulses arrives when the counter is at 1 and reduces the counter to 0. Even if the paired trigger input pulses "split" the subtrahend pair of pulses (in the right-hand clump), the device generates output that is erroneous when held to the standard of an exact difference.

Figure 14: operations of the difference device in violation of constraint